Abstract

A processor includes controller circuitry operative to control the storage of a plurality of separate linked list data structures for protocol data units received by the processor. The linked list data structures are stored in memory circuitry associated with the processor, and the memory circuitry is arranged in a plurality of banks. The plurality of banks are configured to store respective ones of the plurality of separate linked list data structures, such that each of the plurality of banks stores a corresponding one of the plurality of separate linked list data structures. The linked list data structures are accessed in an alternating manner that reduces the likelihood of access conflicts between the banks. The processor may be configured as a network processor integrated circuit to provide an interface between a network and a switch fabric in a router or switch.